17659

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3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(3) Figures to the ***right*** *indicate* ***full*** *marks.*
(4) Use of Non-programmable Electronic Pocket Calculator is ***permissible****.*

Marks

1. A) Solve **any three** : **12**
a) Write VHDL program for 3 bit up counter. **4**
b) Define the terms : **4**
i) Noise margin
ii) Skew.
c) State the use and syntax of : **4**
i) Signal
ii) Constant.
d) Draw two input NAND gate using CMOS technology. Write its truth table. **4**
e) Explain efficient coding style. **4**
B) Solve **any one** : **6**
a) Explain different level of simulation in brief. **6**
b) Explain following statement with example : **6**
i) Process statement
ii) Wait statement.

2. Solve **any four** : **16**
a) Differentiate between BJT and CMOS. **4**
b) List the data types and explain any one. **4**
c) Draw and explain HDL design flow for synthesis. **4**
d) Draw ASIC design flow and explain it. **4**
e) Draw block diagram of Melay and Moore machine and explain it. **4**

3. Solve **any four** : **16**
a) Explain fabrication of N-well process. **4**
b) Define the terms with syntax : **4**
i) Entity
ii) Architecture.

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c) Write VHDL code for D flip-flop. **4**

d) State and explain : **4**
   i) Event scheduling
   ii) Simulation cycle.

e) Differentiate between CPLD and FPGA. **4**

4. A) Solve **any three** : **12**

a) Define the term : **4**
   i) Fan out
   ii) Metastability
   iii) Asynchronous sequential circuit
   iv) Synchronous sequential circuit.

b) Design boolean equation using CMOS : $Z = \overline{AB} + \overline{(C + D)}$. **4**

c) Draw transmission gate. Explain it. **4**

d) Draw neat diagram of architecture of SPARTAN-3 FPGA family and explain it. **4**

B) Solve **any one** : **6**

a) Explain twin tube process with suitable diagram. **6**

b) Draw architecture of CPLD. Explain in brief. **6**

5. Solve **any four** : **16**

a) State the pro's and con's of VHDL. **4**

b) Compare concurrent and sequential statement. **4**

c) Explain estimation of channel resistance of CMOS. **4**

d) Write various factor of selection of FPGA. **4**

e) Design a sequence detector to detect 011 using JK flip-flop using Melay machine. **4**

f) State and explain Delta delay. **4**

6. Solve **any four** : **16**

a) Write VHDL program to implement 4 : 1 mux using case statement. **4**

b) Write VHDL code for full adder. Draw the neat diagram. **4**

c) Differentiate software and hardware description language. **4**

d) Explain CZ method for water processing with neat diagram . **4**

e) Compare between asynchronous and synchronous sequential circuit. **4**

f) Explain zero modelling and sensitivity list. **4**